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Development of INTPIX and CNTPIX Silicon-On-Insulator Monolithic Pixel Devices

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We are developing monolithic pixel detectors utilizing a silicon-on-insulator (SOI) process commercially provided by OKI Semiconductor. Two main pixel sensors, INTPIX and CNTPIX, are being designed as signal integration and counting type devices, respectively. We describe the fabrication results including a buried p-well (BPW) technology recently adopted. The BPW is a breakthrough suppressing the back-gate effect. The radiation resistance of the BPW was also investigated. The ultimate solution to the back-gate effect suppression is stacking of two SOI wafers. We are investigating a 3D process. We also describe the successful results of thinning the wafer to 100 μm.

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1.Introduction

Monolithic devices where readout electronics are integrated on the same chip that contains sensors are very attractive for eliminating the delicate post-process effort in connecting them together which is becoming harder as the pixel size is reduced. With silicon-on-insulator (SOI) technologies, such monolithic devices can be potentially realized. To investigate this possibility, the SOIPIX Collaboration [1] was formed by KEK and Universities in 2005 under the Detector Technology Project [2] of KEK started in 2005. Several works [3]-[5] can be found prior to ours to utilize SOI technologies for monolithic devices. Our technological characteristics are twofold, adoption of bonded SOI wafers fabricated by SOITEC [6] where the resistivity can be chosen optimal for the electronics top silicon and the substrate for thick depleted region, and adoption of fully depleted (FD) 0.20-μm SOI process commercially provided by OKI Semiconductor Co., Ltd.[7] The former is important for high energy charged particle and hard X-ray detections, and in the latter, device fabrication is made reliable under well controlled process procedures.

Figure 1 shows a schematic diagram of our SOI device. A 200 nm thick buried oxide (BOX) layer separates the substrate silicon of typically 260 μm thickness and the top SOI silicon layer of 40 nm thickness. The substrate is Cz grown *n*-type silicon of approximately 700 Ωcm used as the sensitive part. The signal is collected by electrodes created through the BOX layer. The readout CMOS electronics is fabricated in the top silicon of *p*-type and 18 Ωcm resistivity. Connections between CMOS elements are provided by the metal layers on top. The sensors can be biased from the backside or from the top side through ohmic contacts to the substrate.

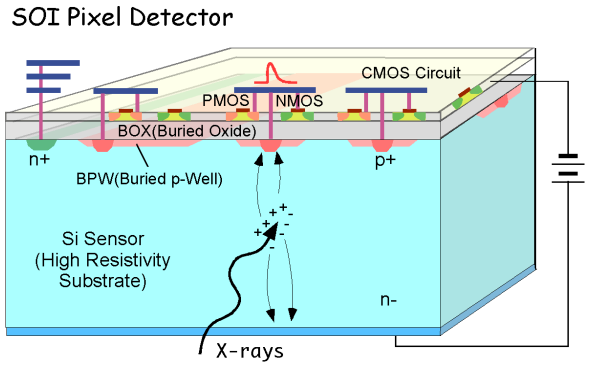

Figure 1: Schematics of SOI monolithic pixel device.

There are several advantages of monolithic SOI devices over hybrid pixel detectors where the electronics and sensor parts are mechanically bonded such as via bump bonds. Since the spacing needed for bump bonding is typically 50 μm, the SOI fabrication is essential to realize devices with smaller pixel sizes. The overall material is reduced in monolithic SOI devices since the substrate for the electronics is the sensitive detector itself. The reduction of material is critical for precision tracking. We are investigating thinner substrates of 100 μm to reduce the material further. The SOI features, high speed, low power dissipation, latchup free, negligible single event upset probability, wide operational temperature range, *etc.* are also realized. The disadvantage, or difficulty, is to suppress the effect of detector bias to the electronics operation (back-gate effect). The total ionization dose (TID) effect is also to be noted since the transistors are fully contained in oxide and there are multiple contributors to the TID effects.

We have implemented a buried p-well (BPW) underneath the BOX, see Figure 1, with its potential controlled externally [8]. The BPW can tie the BOX potential efficiently to the external potential and hence eliminate the back-gate effect. We are also investigating 3D stacking of SOI chips with electronics part moved to a separate stacked layer. Since the

substrates are different for the sensor and electronics, the back-gate effect does not exist in this design.

In Sec. 2, we review our pixel developments. Section 3 details the BPW characteristics. Radiation effects and wafer thinning are described in Secs 4 and 5, respectively. The current status of 3D integration is given in Sec. 6, followed by a summary in Sec. 7.

2. Overview of SOI pixel detector development

We are developing mainly two types of pixel devices, INTPIX and CNTPIX, for signal integration and counting type pixels, respectively [9]. Table 1 summarizes the development history. The fabrications are conducted by Multi-Project Wafer (MPW) runs organized by KEK since FY06. MPW runs allow us to share the costs and, more importantly, accumulate the production experience among the users, which helps to boost the design to a mature level.

We employ a SEABAS DAQ system [10] for signal readout, which communicates with a PC via TCP/IP protocol. Each SEABAS board contains a 65MHz 12-bit ADC and a 4-channel 12-bit DAC. A dedicated sub-board is required for each detector type for signal/command routing and LV/HV distributions, which is connected to the same SEABAS system.

Table 1: Brief history of INTPIX and CNTPIX development

FY05	FY06	FY07	FY08	FY09a	FY09b
TOPPIX	INTPIX1	INTPIX2	INTPIX3	INTPIX3b INTPIX4	INTPIX3c
	CNTPIX1	CNTPIX2	CNTPIX3	CNTPIX4	CNTPIX5
OKI 0.15μm		OKI/OKI Semiconductor 0.20 μm			

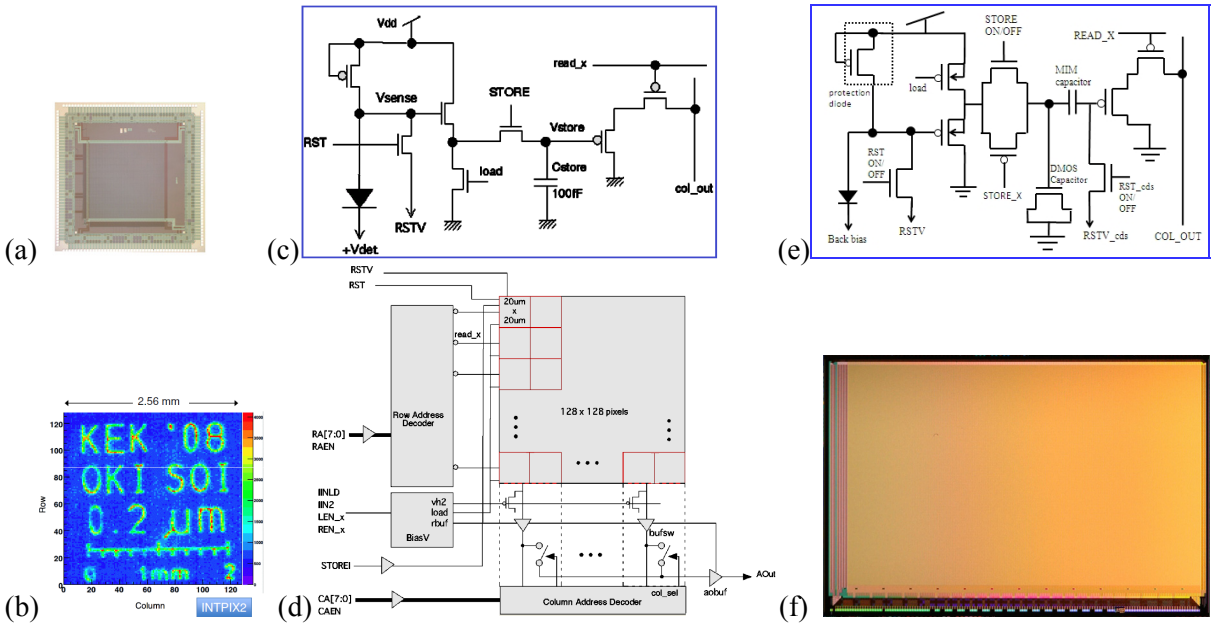

Figure 2: (a) INTPIX3 (outer size: 5×5 mm^2) and (b) a mask image obtained for red laser. (c) APS type on-pixel readout employed in up to INTPIX3, and (d) its peripheral circuit for addressing and analog buffering. (e) CDS on-pixel readout circuit employed in (f) INTPIX4 chip (outer size: 10.2×15.4 mm^2).

2.1 INTPIX

The first pixel PIXELTEG has a 32×32 array of 20×20 μm pixels [11]. The technology of through BOX electrodes fabrication was examined and improved substantially in the next INTPIX1. The INTPIX2 and 3 (see Figure 2(a)) have a 128×128 array of the same pixel size. The diagrams of the on-pixel electronics and the peripheral circuit are shown in Figure 2(c) and 2(d). The mask image to red laser taken with INTPIX2 is shown in Figure 2(b), where the applicable bias was limited to several volts due to the back-gate effects. The BPW was implemented since INTPIX3, whose response at higher biases is discussed in Section 3. The latest INTPIX4 has an array of 512×832 pixels of 17 μm squares. In the INTPIX4, a CDS (correlated double sampling) scheme is added to reduce the noise. This is of prime importance for application to charged particle detection with thinner detectors. The INTPIX4 has 13 parallel analog output chains each handling 512 × 64 pixel signals. New SEABAS-II is under development, which contains multiple ADCs to process INTPIX4 parallel signals.

2.2 CNTPIX

The counting type pixels, CNTPIX, is designed based on the successful Medpix2 chip [12] having double thresholds for signal counting, see Figure 3(a). The analog part contains a charge amplifier with DC leakage current compensation, a test capacitance, and two branches of identical discriminators. The two threshold voltages VthH and VthL are common to all channels with 3 bits each for individual fine threshold adjustment. The hit examined by a double discriminator logic is counted by the 16-bit shift register. The counts during a given integration period are read out one after the other by switching the addresses. An image to X-rays taken with CNTPIX2 that has a 128×128 array of 64 μm square pixels is shown in Figure 3(b). The overall dimensions are enlarged for CNTPIX4 and 5 which have an array of 72×218 pixels. The on-pixel circuit is modified for CNTPIX5 as shown in Figure 3(c). In CNTPIX5, a shaper

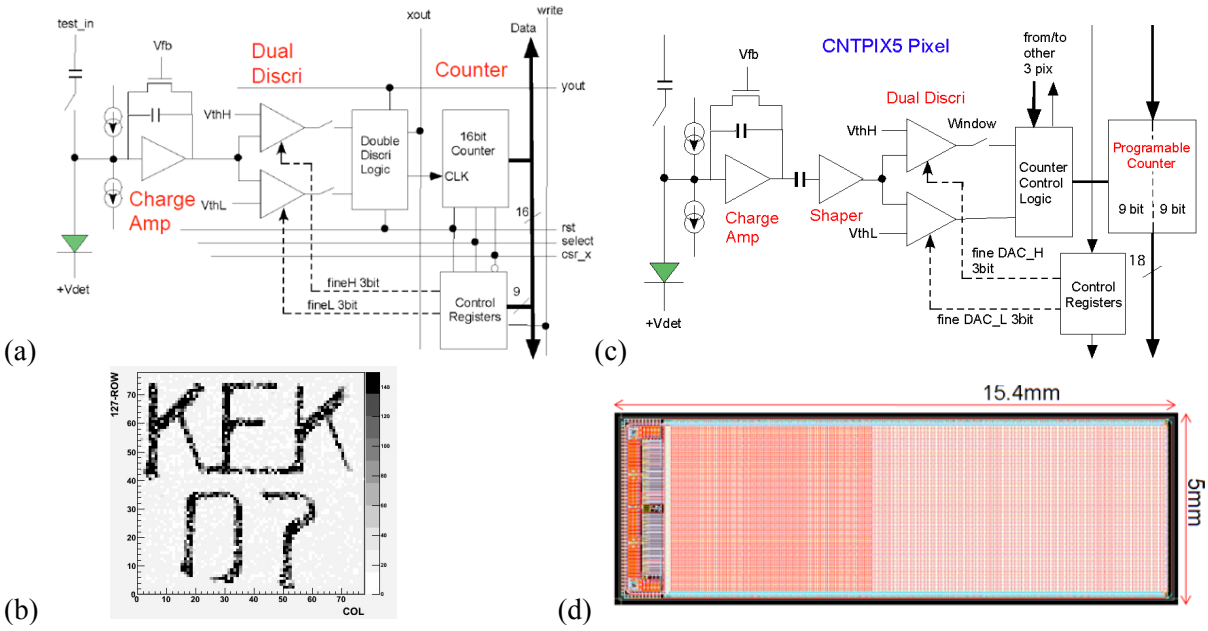

Figure 3: (a) On-pixel readout employed in up to CNTPIX4, and (b) CNTPIX2 brass mask image to 8 keV X-rays obtained with Tint=16ms and HV=20V. (c) Modified on-pixel electronics of (d) CNTPIX5 (5×15.4 mm).

amplifier is added and the counter works as 18-bit or one 9-bit having 2 depths. If 2×2 pixel signals are merged, the counters can be programmed to work as 9-bit with 8 depths.

In the CNTPIX4 and 5 chips, non-active area is minimized in three sides gathering the communication electronics on one side. With this design, multiple chips can be arranged side-by-side or tiled to cover wider areas without introducing significant dead area. SEABAS-II can handle the data in such a configuration.

3. BPW – buried *p*-well

The buried *p*-well, BPW, was introduced to control the potential beneath the BOX and to suppress the back-gate effect. We chose *p* implantation against *n* bulk. Since the BPW implantation is made through the SOI silicon, the concentration is moderate (three orders of magnitude lower than for the source/drain doping) so that the implantation will not change the transistor characteristics significantly. Figure 3 shows the transistor I_d-V_{gs} curves measured in dedicated test transistor elements, demonstrating the effectiveness of the BPW. There is no distortion in the curves up to 100 V applied to the backside, while substantial shifts are observed without BPW even at 5 V and the transistor becomes completely un-operational at 50 V. Additional benefit of the BPW, when it is implanted extending the edges of p^+ implants, is that it relaxes the concentration of electric lines and thus increases the breakdown voltage, the BPW functioning as the graded profile.

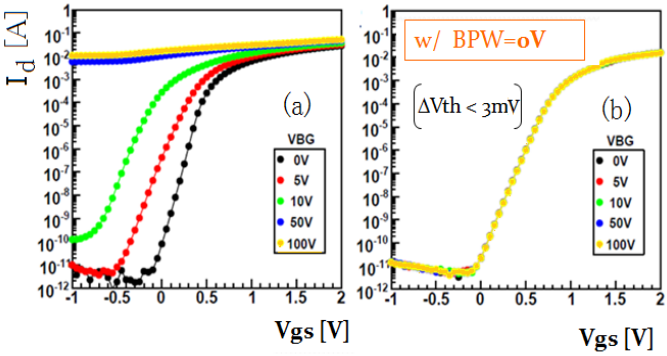

Figure 3: Transistor I_d-V_{gs} curves with V_s=0, V_d=1.8V for several backside voltages from 0 to 100 V. (a) Without BPW, the curve is distorted as the backside voltage is raised, while (b) the curve is constant with BPW set at 0 V.

In INTPIX3 several BPW configurations were examined around the pixels [8]. While the common peripheral circuit is BPW implemented, the pixel area was divided into regions with different BPW shapes. Figure 4 is an example result for two BPW configurations and one without BPW (pixel BPW is shown in light area in the top, where there are four electrodes per pixel), showing collected charge produced by 1064 nm laser as a function of the backside voltage. Since this laser penetrates the Si substrate of 260 μm thickness, the collected charge which is proportional to the depleted depth should be expressed by $\sqrt{V_{back}}$ (dashed

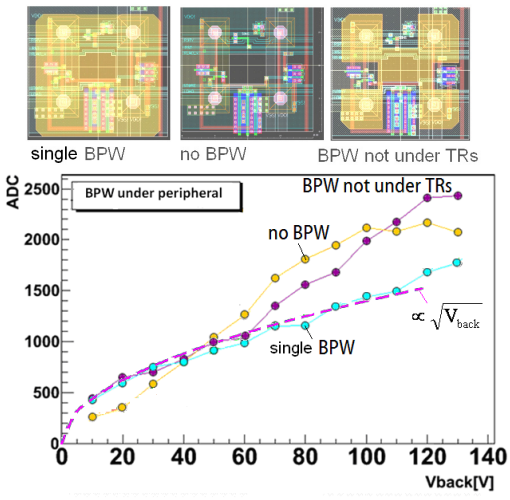

Figure 4: Collected charge as a function of backside voltage. The data are for three BPW (see text) configurations. Dashed curve is an expectation from depleted depth.

curve in the figure). With the configuration where a single BPW (single BPW) covers the whole pixel region, the response curve follows as expected. With the configuration where there is no BPW in the pixel area (no BPW) and where the BPW was implanted avoiding the areas for the transistors (BPW not under TRs), the device responded up to 100 V but the bias dependence does not follow the expected curve. This is explained by that the back-gate effect changes the matching which happens to enhance the response. The two actually saturate at higher biases, and are expected to drop beyond 140 V, although the measurement is limited to 130 V for the maximum applicable voltage. In any configuration, observation of signal at such high biases is due entirely to the BPW implemented under the peripheral circuit, since application of such high voltage was not possible in INTPIX2. We are investigating other BPW configurations to achieve high signal collection efficiently while keeping small cross-talk.

4. Radiation hardness

Evaluation of radiation hardness is in progress using various radiation sources. We report here test results using ^{60}Co γ's and 70-MeV protons. The primary TID effects are evident in the transistor threshold shifts, so dedicated transistor test elements were used for numerical evaluation. The results with cyclotron 70-MeV protons are reported in [13]. The test with ^{60}Co was carried out at JAEA Takasaki Advanced Radiation Research Institute. Seven chips that contain various transistors with and without BPW [13] were irradiated at room temperature at 0.6 - 10 kGy/h up to their scheduled radiation doses, ranging from 0.2 kGy to 500 kGy (SiO_2). All the chip terminals were tied together and grounded. Prior to the transistor parameter characterization, the chips were annealed for 80 min at 60°C in order to compare the results directly with the proton results – This annealing is a recommendation for proton-induced bulk damages to recover the effect of accelerated irradiation.

The I_d-V_{gs} curves measured for V_{ds}=1.8V are shown in Figure 5 for the two groups with and without BPW. The distortion of the curves are evident without BPW as the backside bias is

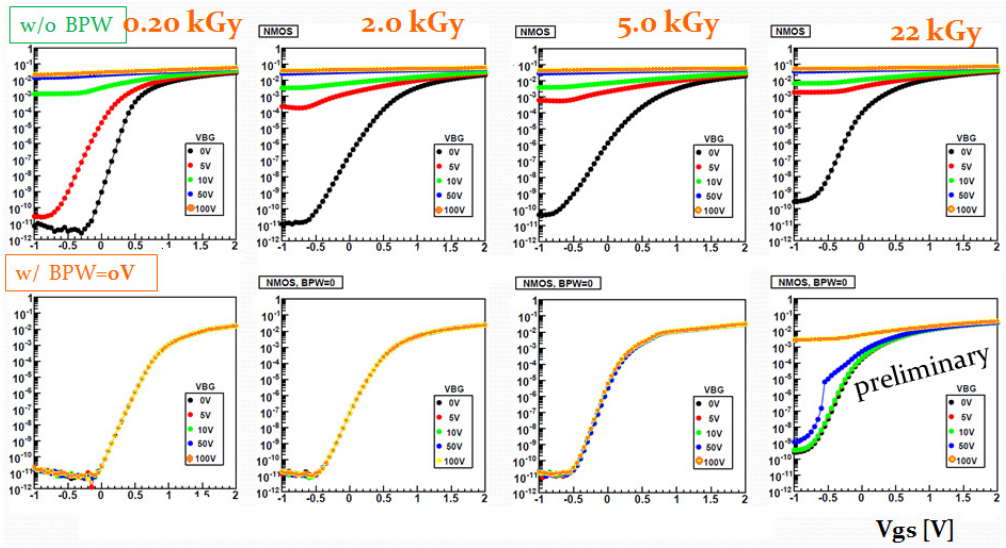

Figure 5: Transistor I_d-V_{gs} curves for several back-side voltages ranging from 0 to 100V. Top row plots are without BPW for ^{60}Co ionization doses 0.20, 2.0, 5.0 and 22 kGy(SiO_2). Bottom row are corresponding plots for transistors with BPW with its potential set at 0 V.

raised (as in Figure 3) and as the dose is increased. The transistors with BPW are stable up to 5 kGy, but the curves were distorted at 22 kGy. In the proton irradiation [13], the I_d-V_{gs} curves were unchanged at 1.3×10^{12} 1-MeV n_{eq}/cm^2, but found to be distorted at 1.2×10^{13} 1-MeV n_{eq}/cm^2, the corresponding ionization dose being 4 kGy by 70-MeV protons. The two results are consistent that the BPW is effective up to several kGy. While the BPW's light doping implantation may explain this, the results may be dependent on the dose rate and further investigation is necessary.

The threshold shifts with the backside voltage set at 0V are compared in Figure 6 for proton and ^{60}Co γ irradiations for NMOS and PMOS transistors. The horizontal ranges are adjusted such that the ionization doses are equivalent between the proton and γ irradiations.

We note the similarity between the two irradiations, NMOS transistors showing a re-bound effect known for bulk MOS devices [14].

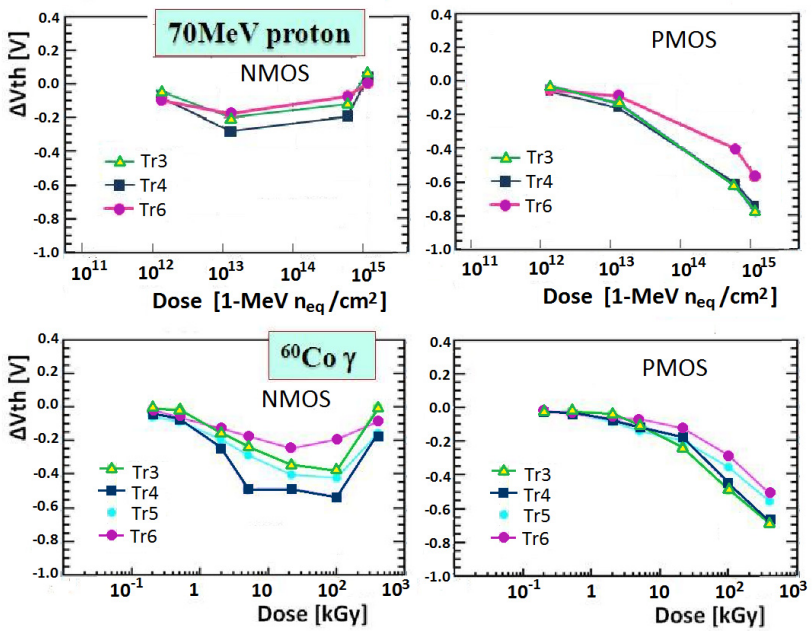

Figure 6: Transistor threshold shifts for NMOS (left) and PMOS (right) transistors. The top plots are for protons and bottom are for γ's.

5. Wafer thinning

OKI Semiconductor starts processing on 8" wafer of 725 μm thickness. They thin the wafer to 260 μm and deposit aluminum on the back surface. With 700 Ω·cm resistivity and a maximum applicable voltage of 140 V, the sensor is not fully depleted with this thickness.

For thinning the wafer further, we adopted the TAIKO process provided by DISCO Co. [15]. In this process, the wafer edge of 3 mm width is left unground. So thinned wafers are self-sustainable and allow us post processing such as backside aluminization. One wafer containing INTPIX2 chips was thinned to 105 μm. Note that INTPIX2 has no BPW. The wafer was cut into blocks and height profile was measured. An example result is shown in Figure 7 for a 4×8 cm block. The profile is convex with the SOI electronics side on top. The maximum

height is 0.4 mm. Other blocks are similar in shape and the heights are characterized by the block size, suggesting these warps are resulting from the difference in the coefficients of thermal expansion between SiO_2 and Si; from the residual strain created at the SOI processing. The I-V curves of several INTPIX2 chips are compared before and after thinning and dicing. As shown in Figure 8, no changes in the leakage current and in the breakdown onset voltages are observed.

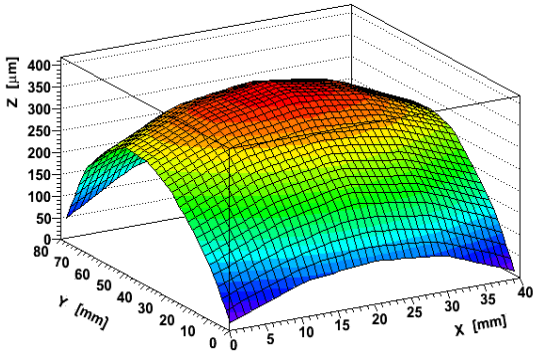

Figure 7: Typical height profile of a 4×8 cm block of 105 μm thick sensors.

Since INTPIX2 has no BPW, substantial back-gate effects are present, as shown in Figure 9 where the response to a halogen lamp measured as a function of the backside voltage is compared between normal and thinned chips. The response, maximum at 5 V bias, decreased to a half at 30 V and 45 V for 105 μm and 260 μm thick sensors, respectively.

Thinning of a wafer containing INTPIX3 is complete and the evaluation is in progress. With INTPIX3 having BPW, the full depletion should be observable.

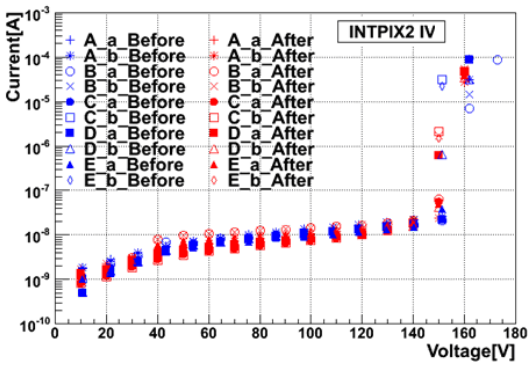

Figure 8: I-V curves of INTPIX2 chips compared before and after thinning.

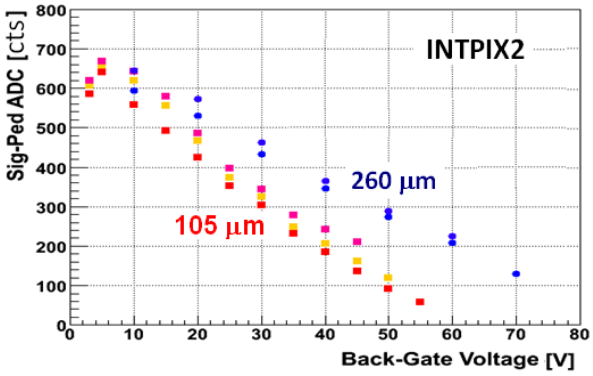

Figure 9: INTPIX2 response to a W lump vs. backside voltage, compared between normal thick (260 μm: circles) and thinned (105 μm: squares) devices.

6. 3D integration

As the performance improvement by shrinking the planar processing rule is approaching to the limit due to the interconnects of finite lengths and the cost of manufacturing itself is becoming high, vertical architectures are becoming viable in recent years.

We are investigating 3D integration in cooperation with Tohoku-MicroTec Co. [16]. The company has key technologies such as deep trench etching in Si and filling with W/poly-Si, and wafer-bonding and thinning [17]. 3D stacking will be an ultimate solution to the SOI back-gate effect by separating the sensor and readout electronics wafers. Although the original benefit of monolithic SOI devices as processed is lost, the SOI features like high speed, low power dissipation, *etc.* can be retained. The compact SOI designs with a regular structure are suitable

for extending in third dimension and two bonding chips can be fabricated with minor design modifications to the present device.

The 3D integration procedure is illustrated in Figure 10. The lower chip is modified to extract the pixel electrodes out to the surface. In the upper chip, with their micro-pads being mirror imaged, pixel signals are received and amplified. The external lines in the lower chip are also handed to the upper chip. At first, both chips are coated with polyimide for smooth surfaces and In/Au micro-bumps are formed. The micro-bumps, 2×2 μm at bottom, are formed by a lift-off method using self-alignment procedure keeping an alignment precision of 0.2 μm. The wafer-bonding technology relies on precision forming of micro-bonds and, after electrical contacts are established, injection of adhesive through narrow gaps for mechanical stability. The top wafer substrate is then etched out to the BOX to reach the metal contacts. Layers of Ti/TiN/Al are sputtered on top to create the metal contacts, followed by SiN deposition for passivation.

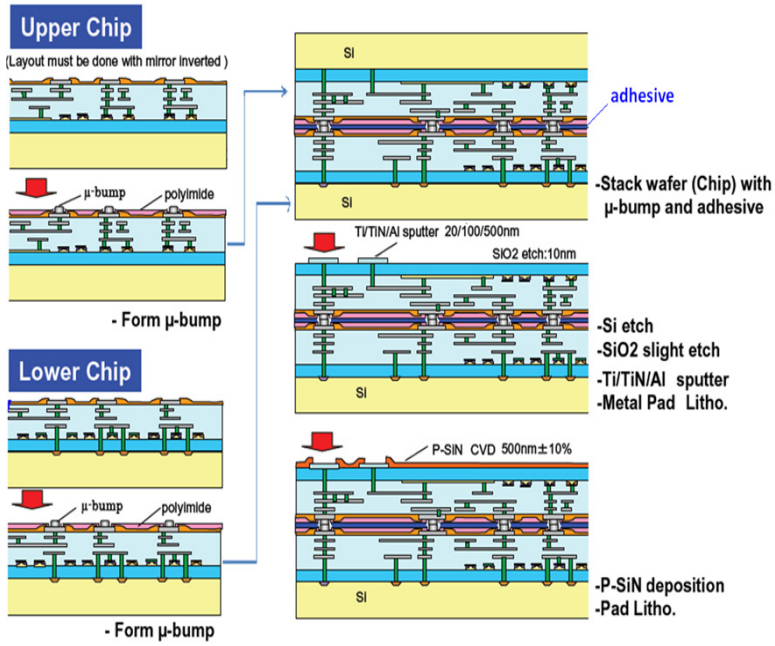

Figure 10: 3D integration of SOI sensors. The upper chip (left top) is flipped and bonded to the lower chip (left above).

The key 3D technologies have been evaluated with SOI test structures on μ-bonding of a minimum bump pitch of 5 μm. The high resistive substrate was found harder to etch down but the process was successful. A cross sectional view is shown in Figure 11. The top silicon is etched to the BOX. The fabrication using real SOI sensors is under way.

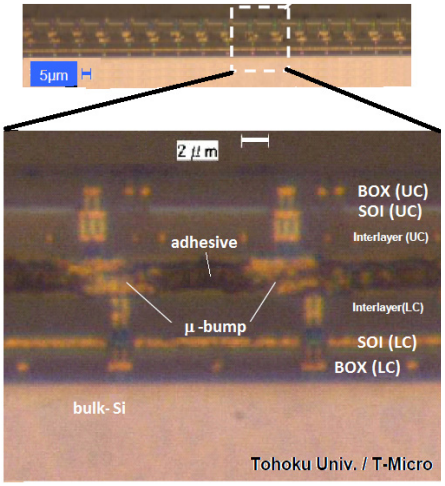

Figure 11: Micro-bump bonding of two SOI wafers.

7. Summary

We have developed monolithic pixel devices suitable for visible light and X-ray detection. New devices have larger sensitive areas, implemented with CDS readout (INTPIX4) and programmable counters with counter control logics (CNTPIX5). The buried *p* well BPW

recently investigated is a breakthrough technology extending the operational voltage with suppressing the back-gate effect. The devices are being examined for charged particle detection. The BPW requires to be optimized in view of charge collection and radiation resistivity. Thinning technology was examined successfully to 100 μm. We are investigating 3D processing which is an ultimate solution to the back gate effect and is expected to enhance the SOI device performance.

Acknowledgments

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