Radiation Effects in Silicon-on-Insulator Devices

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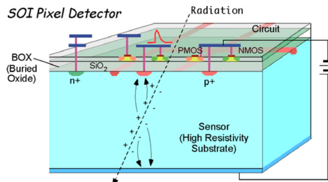
Hiroshima STD7, Aug.29 - Sep.1, 2009

INTRODUCTION

Monolithic pixel sensors are being developed using a Silicon-On-Insulator (SOI) technology. Transistor TEG (test element group) circuits were irradiated with protons to investigate the radiation effects in SOI devices. Threshold voltage shifts are interpreted as caused by charge accumulation in the oxide layers and at the SiO_2-Si interfaces. Buried P-Well can suppress the back-gate effect effectively. The effectiveness of BPW after irradiation is investigated.

1. Monolithic SOI Pixel Detector

Monolithic pixel devices are under development in a commercial SOI process provided by OKI Semiconductor where UNIBOND^{TM} wafers are employed. The wafer allows to choose the resistivity such that the "handling wafer" is high resistive for particle detection while the SOI silicon is optimum for CMOS circuit process.



■ SOIPIX parameters

Process	0.20μm low-leakage fully depleted SOI CMOS: 1 poly Si, 4 metal layers, MIM Capacitors
SOI wafer	(top) 40 nm thick p-type of 18Ωcm; (BOX) 200nm; (handle) 650 nm thick n-type of 700Ωcm
Backside	Thinned to 260mm, 200 nm Al sputtered

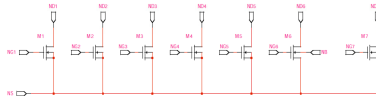
■ OKI 0.20μm FD-SOI processes

Wafer diameter	8"
Gate Length (μm)	0.20
Core/IO voltage (V)	1.8 / 3.3
Gate t_{ox} (nm)	4.5 / 7.0

2. Radiation Effect Evaluation with TrTEG

Radiation effect in the device was evaluated with TrTEGs where basic MOS transistors were fabricated. With TrTEG, we characterized a specific transistor with an HP4145A analyzer selecting a pair of gate and drain terminals.

TrTEGs were irradiated with 70-MeV protons to fluence of 0.13, 1.2, 60, 112x10^{13} 1-MeVn_{eq} /cm^2. The last value corresponds to 0.4 MGy (SiO_2). All the terminals were shorted during irradiation.

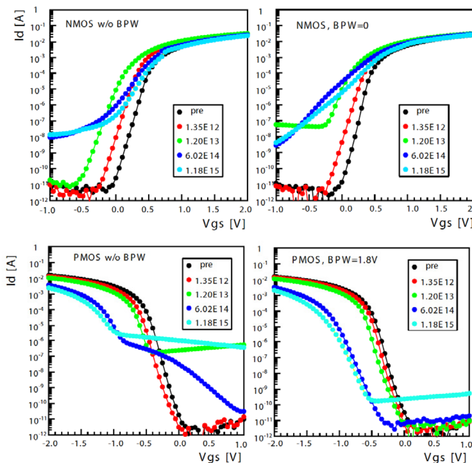


■ TrTEG circuit for NMOS. The sources are common. Similar set is available for PMOS transistors. There are two such groups in a TrTEG, one with BPW and another without.

■ Transistor types (N and PMOS availability)

Tr. number	W/L (μm)	comments
Tr1 (NMOS)	100/0.20	normal V_T core: floating body
Tr2 (NMOS)	100/0.20	low V_T core: floating body
Tr3 (N/PMOS)	175/0.35	High V_T IO: floating body
Tr4 (N/PMOS)	175/0.35	normal V_T IO: floating body
Tr5 (N/PMOS)	175/1.00	normal V_T IO: source tie
Tr6(P), Tr7(N)	100/0.20	normal V_T core: body tie
Tr6 (NMOS)	100/10	depletion mode IO

3. I_d-V_{gs} Curves (proton irradiated)

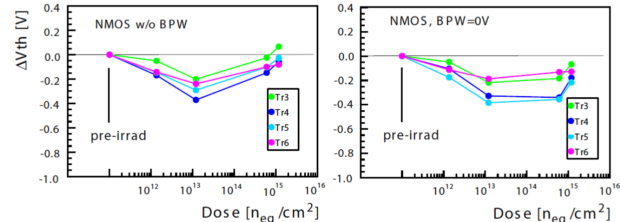


Id-Vgs curves of NMOS transistor Tr4 for four irradiated samples in comparison with non-irradiated, (left) without BPW and (right) with BPW set at ground. Vs=0 and Vd=1.8V. The radiation dose is given in 1-MeV n_{eq} fluence/cm^2.

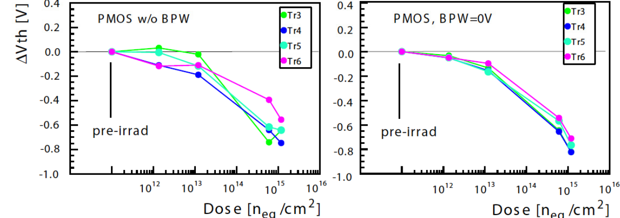
Id-Vgs curves of PMOS transistor Tr4 for four irradiated samples in comparison with non-irradiated, (left) without BPW and (right) with BPW set at 1.8V. Vs=1.8V and Vd=0.

4. Threshold Voltage Shifts at Vback=0V

The threshold voltage is defined where the drain current at I_{ds}=(W/L)x100nA.



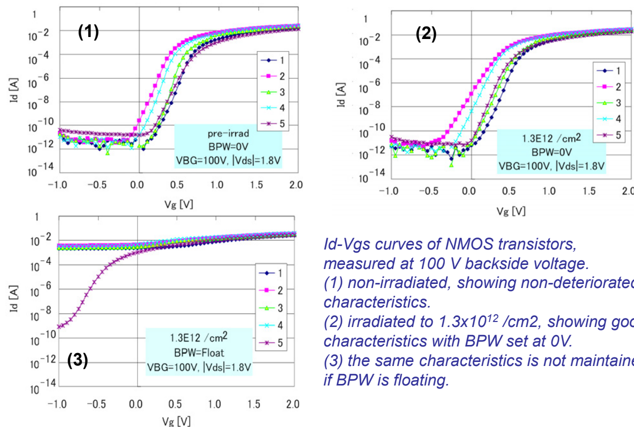
Threshold voltage shifts of NMOS transistors (Tr3-6), (left) without BPW and (right) with BPW set at 0V. Vs=1.8V and Vd=0V. The radiation dose is given in 1-MeV n_{eq} fluence/cm^2.



Threshold voltage shifts of PMOS transistors (Tr3-6), (left) without BPW and (right) with BPW set at 0V. Vs=1.8V and Vd=0V.

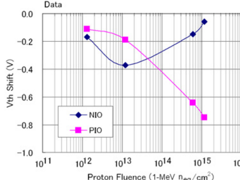
5. Back-Gate Control Method

The operation of SOI transistors is influenced by the voltage applied to the back, known as back-gate effect. In order to suppress this effect, P-Well (BPW) was formed at the BOX-handle wafer boundary.



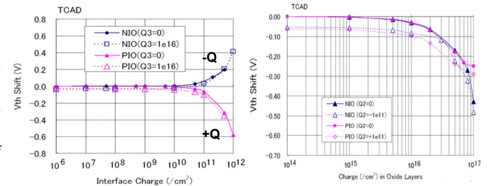
Id-Vgs curves of NMOS transistors, measured at 100 V backside voltage.
(1) non-irradiated, showing non-deteriorated characteristics.
(2) irradiated to 1.3x10^{12} /cm2, showing good characteristics with BPW set at 0V.
(3) the same characteristics is not maintained if BPW is floating.

6. Charge Contribution to V_T Shifts (TCAD)



The difference of V_T shifts between NMOS and PMOS may be attributed to the trapped charges at Si-SiO_2 interfaces and in the SiO_2, the former being negative for NMOS and positive for PMOS.

The individual contributions are simulated with TCAD for Tr4.



Threshold voltage shifts of PMOS and NMOS (Tr4). (top) Data; (right) TCAD - Contributions of trapped charges at interfaces (Q2) for two oxide trap densities (Q3, in cm^{-3}) ; (rightmost) of Q3 for two Q2 values.

Summary

Radiation effects in OKI 0.20μm SOI transistors were evaluated by irradiating TrTEG circuits up to 1.12x10^{15} 1-MeV n_{eq}/cm^2 or 0.6 MGy(SiO_2).

The threshold voltage decreases monotonically with the fluence for PMOS transistors while it re-bounds for NMOS, as expected from different interface charge signs between NMOS and PMOS.

The threshold voltage shifts at 0V back-gate voltage are similar for the devices with and without BPW, as interpreted by radiation induced traps being inherent in the oxide layers and at the interfaces. The BPW effectiveness of suppressing back-gate effects is confirmed up to proton fluence of ~10^{12} /cm^2.