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Thinning of Monolithic Silicon-on-Insulator Pixel Devices

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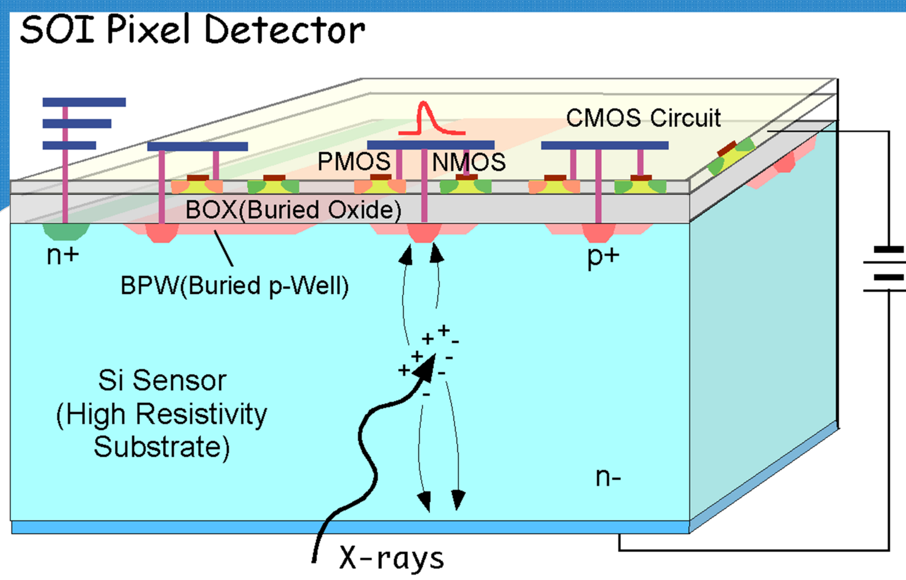

Fig. 1: Schematics of SOI monolithic pixel device.

Introduction

We are developing monolithic pixel detectors utilizing a 0.2-μm fully depleted silicon-on-insulator (SOI) technology commercially provided by OKI Semiconductor. One of the advantages of monolithic SOI devices is reduction of the overall detector material, which is important for precision tacking. The advantage becomes more striking by thinning the sensor. We thinned a wafer to 100 μm by TAIKO process, while 260 μm is our standard thickness. With 100 μm thickness, the device can be fully depleted. This allows us to illuminate from the backside, which helps improve the efficiency and uniformity for visible light/soft X-ray detection. We evaluated the response to infrared and red lasers, and examined the leakage current increase and warp profile.

INTPIX3 Design

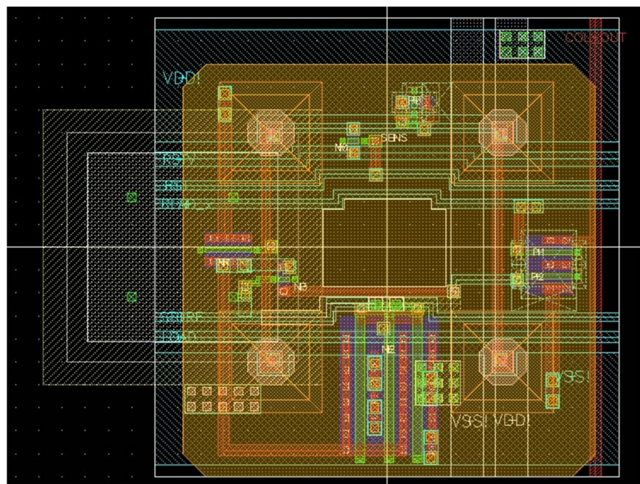
Fig. 2: Pixel layout. The 4 p+ in a pixel are connected together by BPW (yellowish)

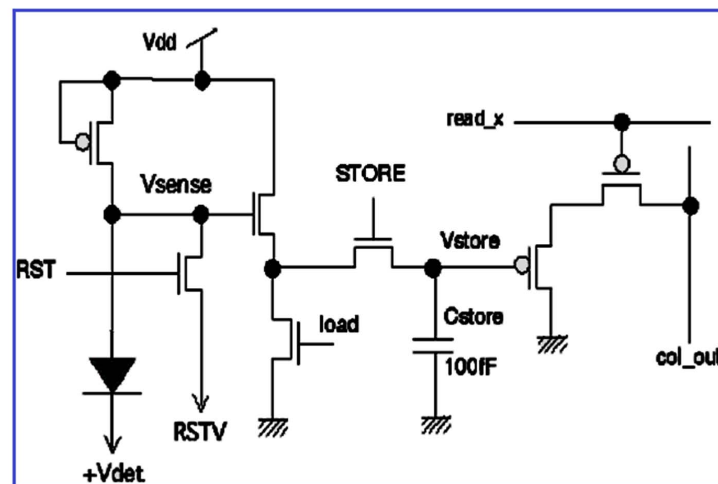

Fig. 3: Diagram of on-pixel circuit.

INTPIX3 is a charge integration type pixel sensor. The pixels, 20x20 μm^2 in size, are arranged in 128x128. The charges stored in 100 fF capacitors are extracted one after the other by selecting addresses (RA[6:0] and CA[6:0] in Fig. 4). The selected signal is digitized by a 65 MHz 12-bit ADC equipped in a SEABAS* board which communicates with a PC via TCP/IP.

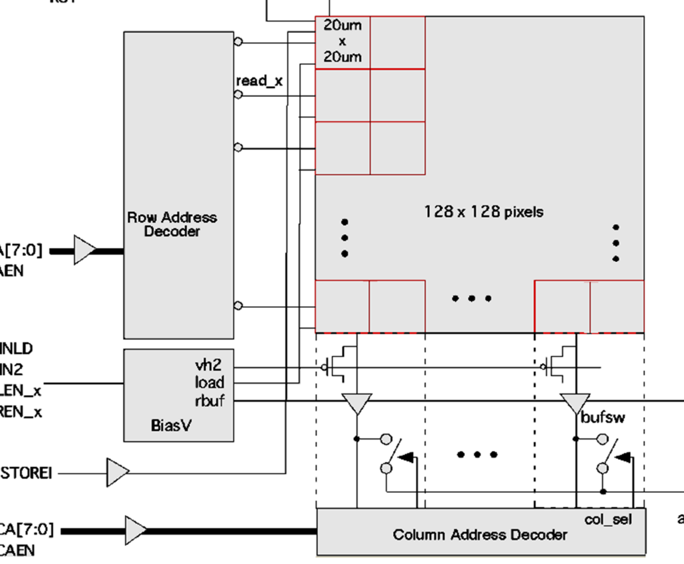

Fig. 4: Peripheral circuit diagram

*T. Uchida and M. Tanaka, *Development of a TCP/IP Processing Hardware, IEEE NS Symposium*, NS33-6, pp1411 – 1414, 2006.

Thinning Process

We adopted TAIKO™ process provided by DISCO Co.$ for thinning. The wafer is mechanically polished with leaving the wafer edge unground. The ground surface was etched chemistry to remove the defects caused by mechanical polishing. . The thinned wafer is self-sustainable, allowing post processing such as aluminization.

$ http://www.disco.co.jp/jp/solution/library/taiko.html.

I-V Curve

The I-V curves of several INTPIX3 chips are compared before and after thinning and dicing. The location of the chips is shown in Fig. 5. Noticeable changes are not observed (Fig. 6) in the breakdown onset voltage and in the leakage current. Small position dependence on wafer is observed (Fig. 7,8).
INTPIX3: overall area 25 mm², pixel area 6.3 mm².

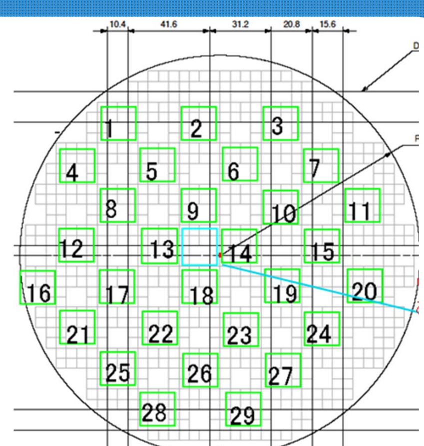
Fig. 5: Measured chip location (before:1-29 after:8-29).

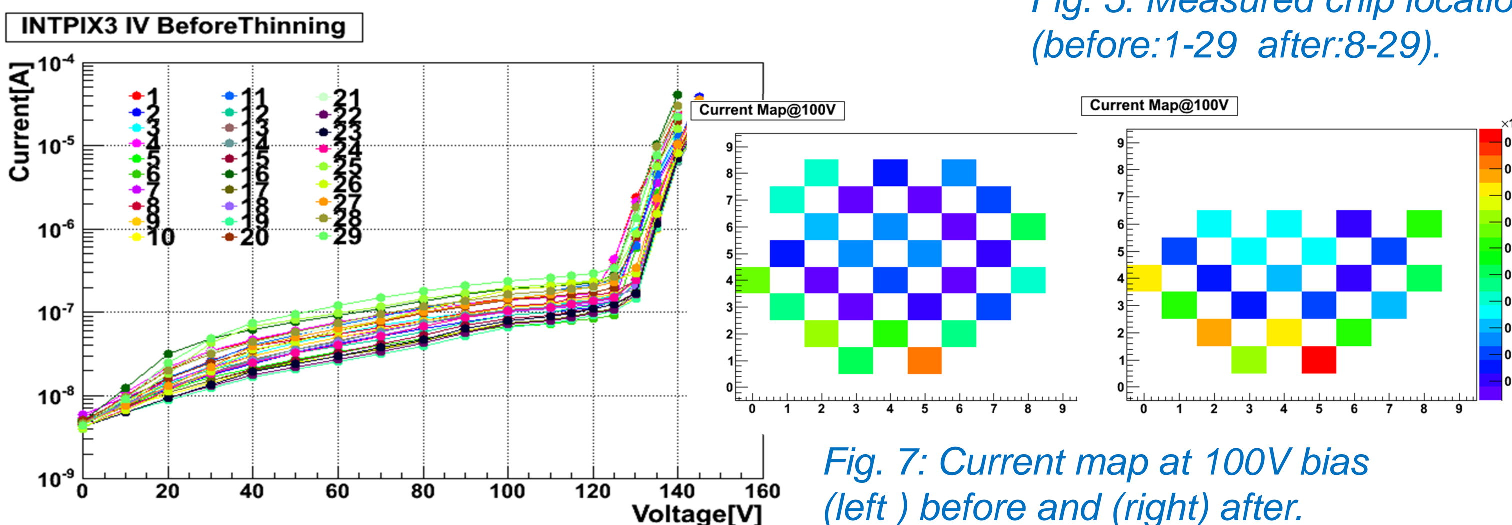

Fig. 7: Current map at 100V bias (left) before and (right) after.

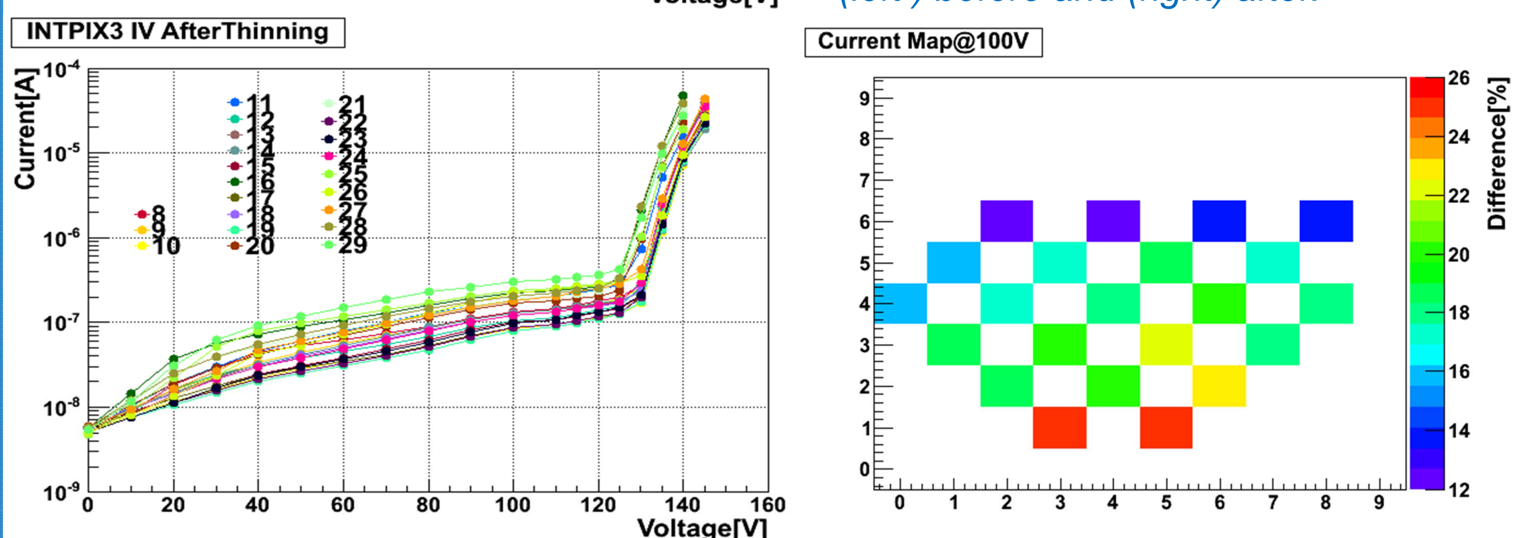

Fig. 6: I-V curves at 20ºC (top) before and (above) after thinning,.

Fig. 8: Relative difference of leak current (after-before)/before at 100 V. The value is about 10 ~ 25 %.

Response to IR/RED Laser

We estimated the depletion depth from the collect charge for 1064 nm laser as a function of the bias voltage. Since this laser penetrates the Si substrate, the collected charge, which is proportional to the depleted depth, should be expressed by $\sqrt{V}$.

FRONT ILLUMINATION:
IR laser was concentrated in a window (Fig. 9), no metal region to allow illumination from the electronics side (see also Fig.2). The collected charge increases linearly with $\sqrt{V}$ for 260 μm thick sensor (Fig. 10), while it saturates above 90 V for 100 μm thick sensor, showing a full depletion.

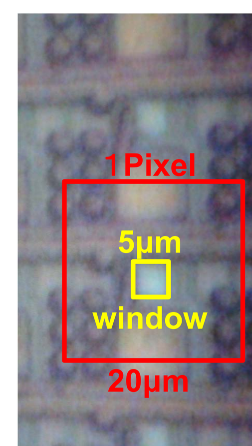

Fig. 9: (red) a pixel, (yellow) a window.

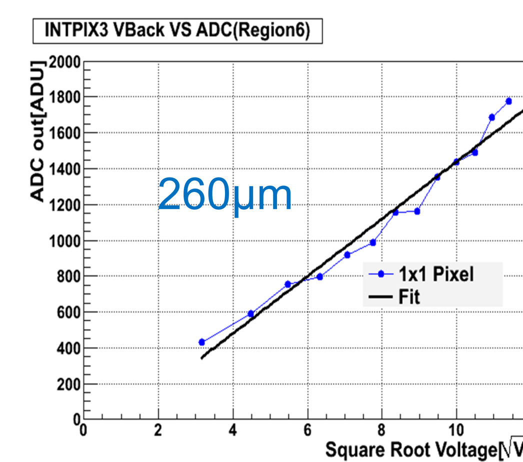

Fig. 10: Collected charge as a function of square root of bias. The sensor is 260 μm thick

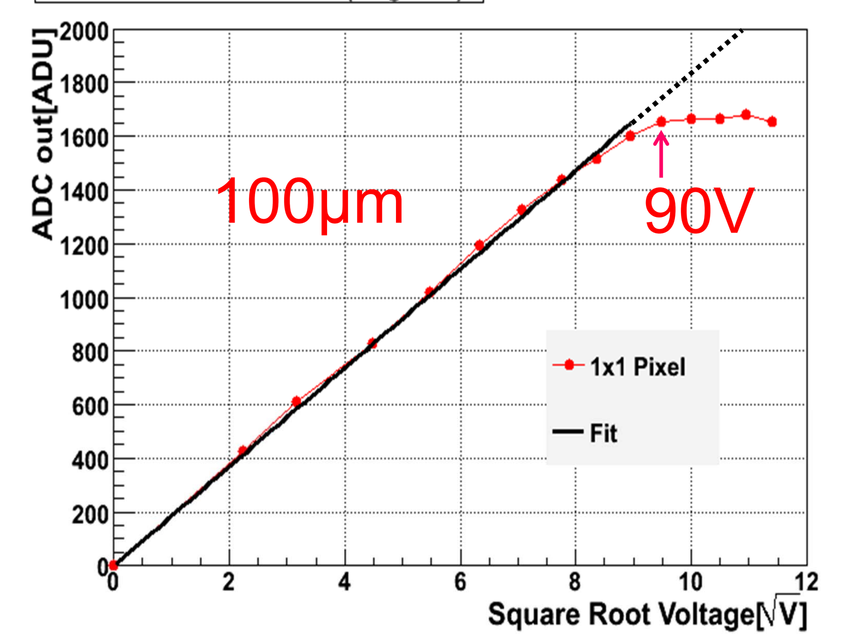

Fig. 11: Collected charge as a function of square root of bias voltage. The sensor is 100 μm thick.

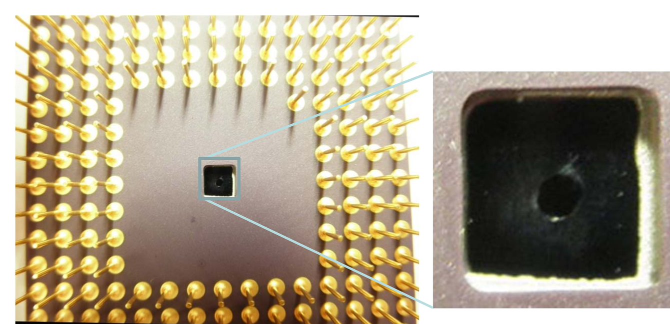
Fig. 12: Backside of the packaged thin INTPIX3. Holes are made through the ceramic and Al.

BACK ILLUMINATION:
For IR laser, the response for back illumination is similar (Fig. 13) to that for front illumination. As a comparison, we incident red laser ($\lambda = 634$ nm) from the backside. Red laser is absorbed at the surface and no substantial charge should be collected unless the device is fully depleted. The result shown in Fig. 13 supports this expectation. However, a fraction of charge is collectable at voltages below full depletion, suggesting fraction of carriers diffuse through the non depleted layer. Fig.14 shows the outputs from the pixels in the area extending to the area covered by aluminum.

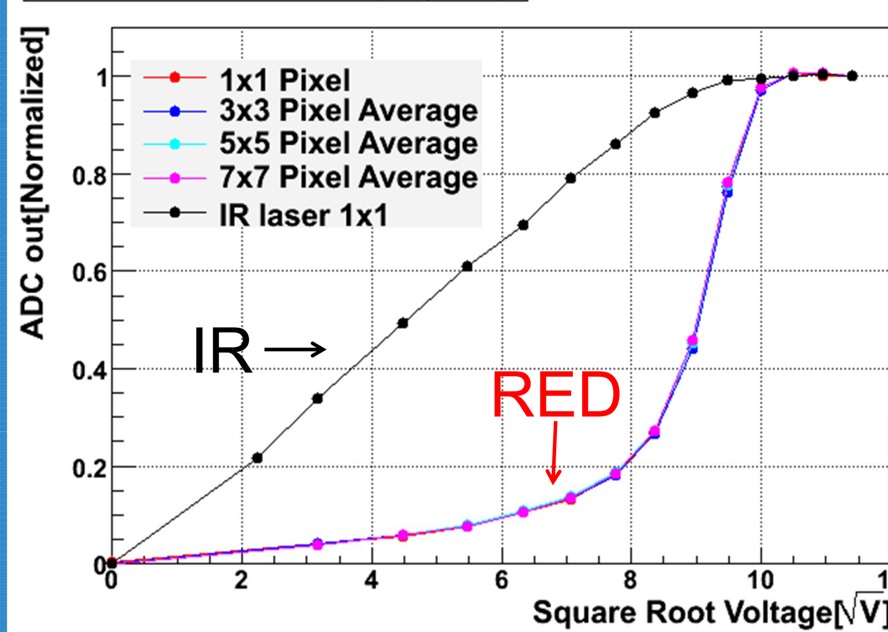

Fig. 13: Collected charge as a function of square root of bias voltage. The sensor is 100 μm thick. The data are normalized at the values at 130 V.

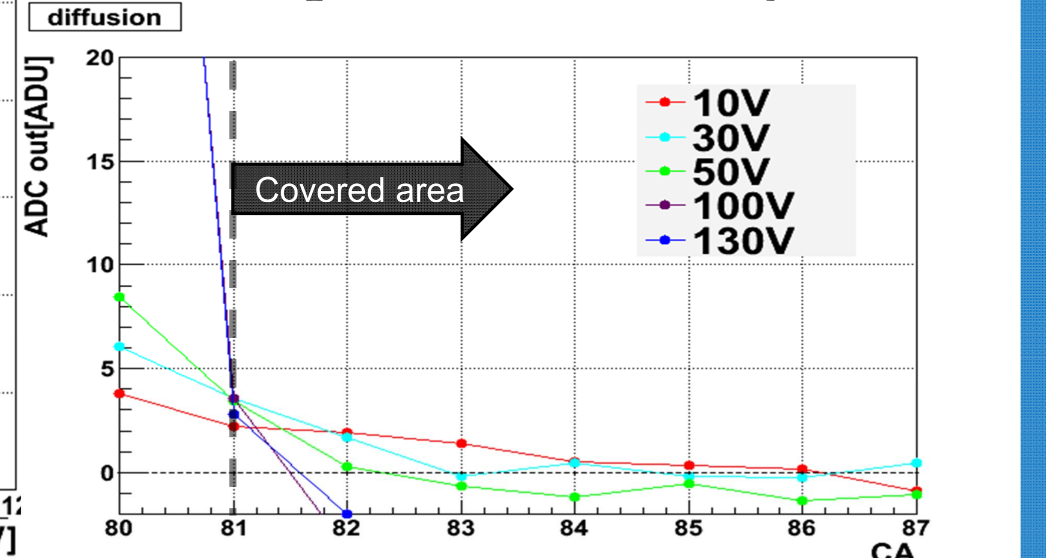

Fig.14: Effect of diffusion measured for red laser illuminated from the back. The abscissa unit is 20 μm. The luminous output at 100V is about 200 ADU.

Warp of Thinned Wafer

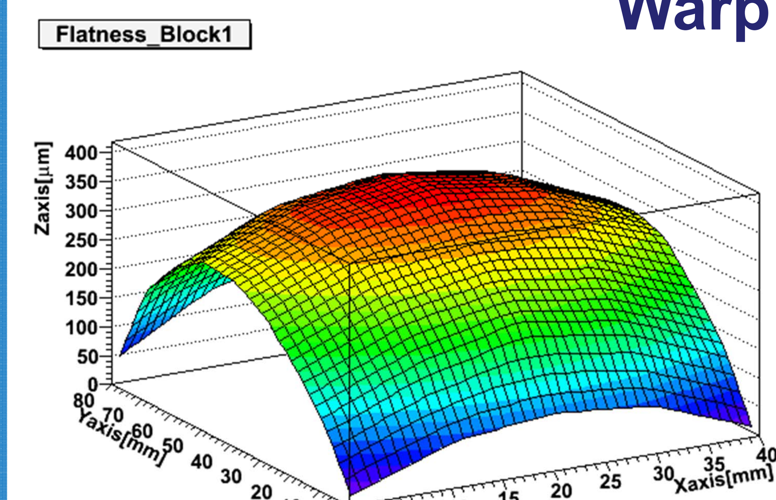

Fig. 15: Typical height profile of a 4 x 8 cm² block of 100 μm thickness.

The thinned wafer was cut into blocks and the height profile was measured. An example result is shown for a 4×8 cm² block (Fig. 15). The profile is convex with the SOI electronics side on top with the maximum height of 0.4 mm.
Other blocks are similar in shape and the heights are characterized by the block size. These warps are considered to result from the residual strain created at the SOI processing due to the difference in the coefficients of thermal expansion between SiO_2 and Si.

Summary

We successfully thinned INTPIX3 SOI monolithic devices to 100 μm.

- We observed no changes in breakdown onset voltages and small changes in the leakage current by thinning procedure.
- Some warp is evident for thinned wafer due to residual strain from the SOI process. The magnitude of the warp should be manageable.
- Full depletion voltage of 90 V is evaluated from the response to infrared laser, and to red laser illuminated from the back.